REMARKS

These remarks are in response to the Final Office Action having a mailing date of July 1, 2005. Claims 1-19 are pending in the present Application. Claims 1-19 are rejected. Claims 1-19 remain pending in the present application. For the reasons set forth more fully below, Applicants respectfully submit that the claims as presented are allowable. Consequently, reconsideration, allowance, and passage to issue are respectfully requested.

In the event, however, that the Examiner is not persuaded by Applicants' arguments, Applicants respectfully request that the Examiner enter the arguments to clarify issues upon appeal.

Present Invention

An application specific integrated circuit (ASIC) is disclosed. The ASIC includes a standard cell. The standard cell includes a plurality of logic functions. The ASIC also includes at least one bus coupled to at least a portion of the logic functions and a plurality of internal signals from the plurality of logic functions. Finally, the ASIC includes a filed programmable (FP) function coupled to the at least one bus and at least a portion of the plurality of internal signals. The FP function provides access to internal signals for observation and control without requiring input/output (I/O) pins to access the internal signals.

An ASIC using a filed programmable gate array (FPGA) function within a standard cell design is utilized to create an internal-to-the-ASIC bridging of internal signals to observe and control of the internal signals of the ASIC. By the placement of the logic, which expresses a test program into the FPGA function and manipulates the I/O pins and/or other functional entities of interest, the ASIC function and/or surrounding logic can be easily verified. In addition, through

this system, internal and/or system (external-to-the ASIC) conditions can be observed. Furthermore, a sequence of resets to different functional blocks can be executed utilizing a system and method in accordance with the present invention. Finally, through this system the end user of the ASIC could write their own error condition correction FPGA code which would communicate using protocols of the existing system error condition architecture.

Claim Rejections - 35 U.S.C. §112

The Examiner has stated:

Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claims 1, 13, and 15, due to the current amended portions and apparent contradictions as recited above are rejected as being indefinite for failing to particularly point out and distinctly claim the subject matter.

Claims 2-12, 14, and 16-19 are dependent upon the independent claims 1, 13, and 15 and thus inherit the 35 USC 112 second paragraph issues of the independent claims.

Since the amendments to the claims render the claims indefinite, the previous rejection is maintained.

Response to Amendment

Claims 1, 13, and 15 have been amended to add the negative limitation "without requiring input/output (I/O) pins to access the internal signals". Although the MPEP does allow for negative limitations as described in MPEP 2173.05(i).

The current view of the courts is that there is nothing inherently ambiguous or uncertain about a negative limitation...

This being stated, the examiner would like to point out that although there is no literal basis in the specification, reading the parts of the specification as pointed out by applicant (Current amendment; page 6, lines 5 and 6), if read in this context, seem to contradict with other segments of the specification (Abstract, page 4, line 20 through page 5, line 1, page 15 lines 7-12). In statements such as: "An ASIC using FPGA function within a standard cell design is utilized to create an internal-to-the-ASIC bridging of internal signals to observe and control of the internal signals of the ASIC. By the placement of logic, which expresses a test program, into the FPGA function that manipulates the I/O pins and/or other functional entities of interest, the ASIC function and/or surrounding logic can be easily verified."

Applicant appears to be arguing that the observed and controlled signals are not sent external to the circuit (page 8 of current amendment). This being the case, "By the placement of logic, which expresses a test program, into the FPGA function that manipulates the I/O pins and/or other functional entities of interest..." would seem unnecessary. However, this argument also appears to contradict the aspects of dependent claim 3 which states: "the signal connector function comprises a first

> **logic for providing an external I/O function and a second logic which is in communication with the first logic that selects the appropriate internal signals for external observation and control."**

Applicants respectfully submit that independent claims 1, 13, and 15, as amended in the Amendment filed April 27, 2005, are definite under 35 U.S.C. 112, second paragraph. Applicants respectfully submit that the claimed feature, "a field programmable (FP) function," "wherein the FP function provides access to internal signals for observation and control without requiring input/output (I/O) pins to access the internal signals," as recited in independent claims 1, 13, and 15, are proper. While the Examiner has stated that the MPEP does allow for negative limitations as described in MPEP 2173.05(i), the Examiner has also asserted:

> ...reading the parts of the specification as pointed out by applicant (Current amendment; page 6, lines 5 and 6), if read in this context, seem to contradict with other segments of the specification (Abstract, page 4, line 20 through page 5, line 1, page 15 lines 7-12).

However, Applicants respectfully submit that the support for the amendments provided on page 4, lines 7-10; page 11, lines 17-18; and page 12, lines 8-11, of the specification does not contradict with other sections of the specification. Those sections quoted by the Examiner state:

> An ASIC using a field programmable gate array (FPGA) function within a standard cell design is utilized to create an internal-to-the-ASIC bridging of internal signals to observe and control of the internal signals of the ASIC. By the placement of logic, which expresses a test program, into the FPGA function that manipulates the I/O pins and/or other functional entities of interest, the ASIC function and/or surrounding logic can be easily verified. (Abstract, page 4, line 20 through page 5, line 1, page 15 lines 7-12)

The claim specifically states that I/O pins are not required to "access internal signals," which is supported on page 4, lines 7-10; page 11, lines 17-18; and page 12, lines 8-11, of the specification. The fact that I/O pins may be manipulated does not contradict with the claim or these sections, because the I/O pins, if manipulated, are not used to access the internal signal. Instead, the I/O pins are merely manipulated to test the ASIC function and/or surrounding logic so that the "ASIC function and/or surrounding logic can be easily verified" (page 4, line 20, to

page 5, line 1). As quoted above, these sections of the specification clearly state that the FPGA function is "within a standard cell design" and that the logic, which expresses a test program, is placed "into the FPGA function" that manipulates the I/O pint and/or other functional entities of interest." As the ASIC function and/or surrounding logic is exercised, the present invention enables non-I/O accessible points of interest to be tested. This is beneficial because ASIC tests may be performed in the field if needed without requiring an external ASIC tester (page 12, lines 8-11). In other words the I/O pins may be relevant to testing the ASIC function and/or surrounding logic in that the I/O pins are exercised by the FPGA function, but the I/O pins are clearly not required "to access internal signals" for observation and control.

The Examiner has suggested that Applicants' arguments on page 8 of the Amendment filed on April 27, 2005 appears to contradict the aspects of dependent claim 3. The Examiner may be referring to Applicant's comment that the cited reference (Shen) teaches an I/O interface that can "transfer the data to a debugging workstation" (column 4, lines 55-58) and that "software can display any of the internal signals that are connected to the I/O of the FPGA core" (column 5, lines 33-36). However, the fact that I/O pins are not required to access internal signals, as recited in the present invention, does not contradict dependent claim 3. Claim 3 recites that a first logic "for providing an external I/O function." As describe above, the I/O function may be relevant to testing the ASIC function and/or surrounding logic in that the I/O pins are exercised by the FPGA function, but the I/O pins are clearly not used to "access internal signals."

Dependent claims 2-12, 14, and 16-19 depend from claims 1, 13, and 15, respectively. Accordingly, Applicants respectfully submit that dependent claims 2-12, 14, and 16-19 are also definite under 35 U.S.C. §112, second paragraph, for at least the same reasons as claims 1, 13, and 15.

Claim Rejections - 35 U.S.C. §102

The Examiner has stated:

> **Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Shen et al. U.S. Patent No. 6,829,751.**
>
> **As per claim 1, Shen et al. teaches providing a method and/or architecture for implementing a diagnostic architecture using an (*field programmable function*) FPGA core in a system on-chip design that can (i) ease bringing up, verification and debugging by providing interconnection and programming options; (ii) *observe* important signals while the chip is running under a normal mode; (iii) run at a single step mode while under the control of the FPGA core; (iv)display appropriate signals on a debugging workstation, allowing many debugging features to be supported such as: (a) triggering and tracing based on *internal signals*, (b) dynamically changing host register values and (c) providing complex monitoring functions (*observation and control*), since the (*field programmable function*) FPGA is programmed; (v) reduce debugging/verification time and/or (vi) improve product time to market. (Column 1 line 56 through column 2 line 12) The register block communicates with the FPGA core through a bus (*at least one bus coupled to at least a portion of the logic functions*). Similarly, the register block (*standard cell*) can also communicate with the FPGA core through other busses. The buses can be implemented as multi-bit buses or can also be implemented as single bit buses, if appropriate. Additionally, the buses can also be implemented as bidirectional buses. The FPGA core can communicate with the control block (*standard cell*) through a bus. The FPGA core can communicate through a number of I/O pins over a bus. (Fig 2, column 3 lines 13-31) By using the FPGA core to implement such chip diagnostics, simultaneous probing of internal signals can be achieved while the system is running under predetermined conditions (e.g., a normal mode of operation). (Column 3 lines 32-42 figure 2) This circuit can also be implemented by the preparation of (*application specific integrated circuit*) ASICS, FPGAs, or by interconnecting an appropriate network of conventional component circuits. (Column 5 lines 54-58) The circuit can provide a FPGA core in an ASIC architecture that eases chip bring up, verification and debugging by interconnection and programming options. This allows important signals of a chip to be observed while the chip is running under a normal mode by connecting the internal signals to the FPGA core I/O. This allow all the signals of the chip to be displayed while the chip is running under a single step mode by allowing a FPGA core to control the chip. (Column 6 lines 18-30)...**

Applicant respectfully disagrees with the Examiner's rejections. Shen discloses diagnostic architecture using a FPGA core in a system-on-a-chip design. The architecture includes a system for designing an integrated circuit (IC). The system includes a circuit and a programmable portion used for diagnostics and finding bugs. The circuit includes a functional portion and a logic portion that may be connected to the functional portion. The logic portion includes one or more interfaces. The programmable portion may be configured to detect, correct

and/or diagnose errors in the logic portion through the one or more interfaces. Up to 1K of internal signal probing can be supported simply by directly connecting the signal to the I/O_PINS of the FPGA core. Also, important signals of a chip can be observed while the chip is running under a normal mode by connecting the internal signals to the FPGA core I/O. (Column 3, lines 58-61, column 6, lines 25-29, and the Abstract.)

As argued in the Amendment filed on April 27, 2005, Shen does not teach or suggest monitoring internal signals "without requiring input/output (I/O) pins to access the internal signals," as recited in independent claims 1, 13, and 15. Instead, Shen explicitly teaches that "up to 1K of internal signal probing can be supported simply by directly connecting the signal to the I/O_PINS of the FPGA core" (column 3, lines 58-61). Furthermore, while Shen teaches simultaneously probing multiple internal signals by utilizing a scan chain (column 6, lines 45-47), Shen also teaches that when collecting data using the scan chain, the "I/O interface may then transfer the data to the debugging workstation" (column 4, lines 55-58). Shen further states that "software can display any of the internal signals that are connected to the I/O of the FPGA core" (column 5, lines 33-36), and that important signals of a chip can be "observed while the chip is running under a normal mode by connecting the internal signals to the FPGA core I/O" (column 6, lines 25-29). In other words, Shen requires I/Os in order to debug internal signals using the debugging workstation, to display internal signals using software, and/or to observe internal signals. Nowhere does Shen teach or suggest monitoring internal signals "without requiring input/output (I/O) pins to access the internal signals," as recited in the present invention.

Therefore, Shen does not teach or suggest the present invention as recited in independent claims 1, 13, and 15, and these claims are allowable over Shen.

Dependent claims

Dependent claims 2-12, 14, and 16-19 depend from independent claims 1, 13, and 15, respectively. Accordingly, the above-articulated arguments related to independent claims 1, 13, and 15 apply with equal force to claims 2-12, 14, and 16-19, which are thus allowable over the cited reference for at least the same reasons as claims 1, 13, and 15.

Conclusion

In view of the foregoing, Applicants submit that claims 1-19 are patentable over the cited reference. Applicants, therefore, respectfully request reconsideration and allowance of the claims as now presented.

Applicants' attorney believes that this application is in condition for allowance. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,

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Date

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